Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **DATA B**
2. **OUTPUT QB**
3. **OUTPUT QA**
4. **DOWN COUNT**
5. **UP COUNT**
6. **OUTPUT QC**
7. **OUTPUT QD**
8. **GND**
9. **DATA D**
10. **DATA C**
11. **LOAD**
12. **CARRY**
13. **BORROW**
14. **CLEAR**
15. **DATA A**
16. **VCC**

**.081”**

**.081”**

**2 1 16 15**

**14**

**13**

**12**

**11**

**7 8 9 10**

**3**

**4**

**5**

**6**

**193C**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 193C**

**APPROVED BY: DK DIE SIZE .081” X .081” DATE: 2/18/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54LS193**

**DG 10.1.2**

#### Rev B, 7/19/02